A 9 GHz OSCILLATOR STABILIZED WITH A STW DELAY LINE

Rolf Hügli and Urs Lott

Swiss Federal Institute of Technology (ETH) Zürich,
Institut für Feldtheorie und Höchstfrequenztechnik,
CH-8092 Zürich, Switzerland

ABSTRACT

This paper presents a STW-stabilized X-band oscillator. The main feedback oscillator circuit consists of a third harmonic STW delay line at 2.25 GHz, a two stage amplifier and a diplexing network. The second stage of the amplifier in the oscillator loop doubles the frequency from 2.25 GHz to 4.5 GHz. An additional 4.5 GHz to 9 GHz MESFET doubler is integrated on the same substrate. The oscillator delivers 5 mW of output power. Phase noise is at least -90 dBc/Hz down at 20 kHz from the carrier.

I. INTRODUCTION

Surface transverse waves (STW) and harmonic interdigital transducers allow the fabrication of delay lines for frequencies up to 3 GHz with standard optical lithography. With these devices, low-noise oscillators in the lower GHz region (needing no multiplier chain) have been described [1,2].

The high operating frequency of harmonic STW delay lines is an advantageous basis for the design of stable X-band sources: A frequency multiplication by 4 to 6 is sufficient. This increases the broadband noise floor by only 12 to 16 dB.

In this paper, a compact 9 GHz oscillator using only three transistors and a small number of passive components is described.

Fig. 1 shows the block diagram of the realized circuit. The STW delay line at 2.25 GHz determines the short term stability of the circuit. The loop amplifier consists of two transistors. The first transistor works as a high gain linear amplifier, the second stage amplifies the fundamental and doubles it to 4.5 GHz. A diplexing network separates the two frequencies. The 4.5 GHz signal then passes an additional MESFET frequency doubler.

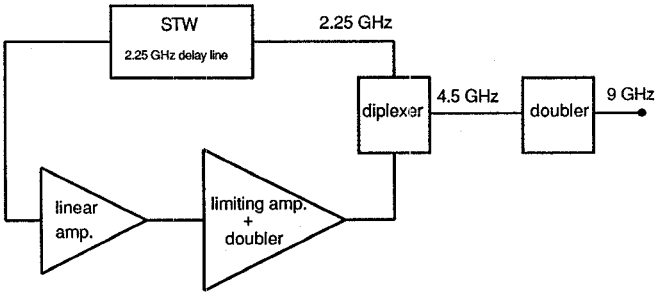

Figure 1: The block diagram of the 9 GHz STW oscillator

Section II explains the design of the feedback oscillator. Section III describes the output doubler. Section IV contains the measurements of the complete circuit.

II. OSCILLATOR WITH STW DELAY LINE

1. Delay Line

The STW delay line is made on AT cut (35.5° rot Y) quartz. It consists of two identical, unweighted bidirectional transducers and a shorted "energy trapping" grating in between. Each transducer has 100 electrode pairs with split electrodes (0.85 µm wide) for third harmonic operation. Q value and insertion loss of the delay line are important parameters for the performance of the oscillator. A high Q value calls for a long propagation distance of the wave. But a longer propagation path increases insertion loss, particularly at frequencies above 1 GHz. As a compromise, a Q value of 1200 has been chosen.
To minimize the insertion loss further, a thin metallization [3] of 30 nm was used. Fig. 2 shows the frequency and phase response of the unmatched device. The unmatched insertion loss is 22 dB.

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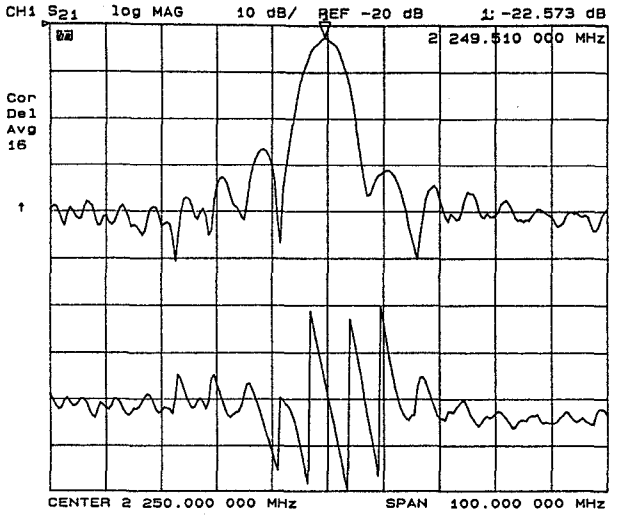

Figure 2: The frequency and phase response of the 2.25 GHz STW delay line

The delay line is mounted directly on the MIC substrate. No hermetic packaging is used in the prototype circuit. Fig. 3 shows the mounting of the device with the bonding wires connecting the microstrip lines.

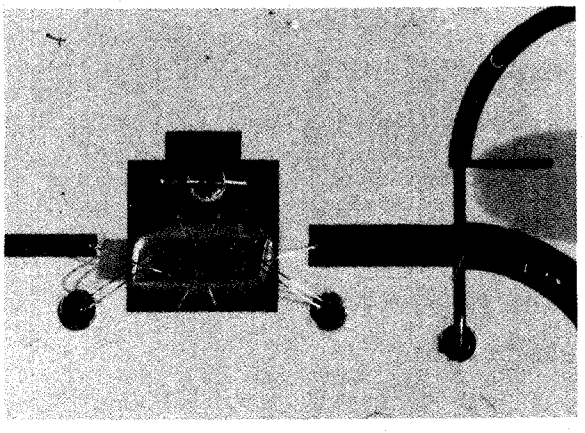

Figure 3: The mounting of the delay line in the MIC circuit

2. Amplifier Stages

The first stage of the amplifier uses a dual gate MESFET (DXL 2704A). It is biased for linear operation (4V, 25 mA) and matched for high gain (19 dB).

The second transistor has three different functions: amplification, limiting of the fundamental and producing a strong second harmonic. In this stage, a bipolar transistor (HXTR 3675) is used to minimize the AM noise contribution, which will be partially converted to PM noise by the limiter action.

An important design trade-off is the partitioning of the output power between the fundamental (2.25 GHz) and the second harmonic (4.5 GHz). To get a low-noise oscillator, a high power level at the fundamental has to be fed back through the SAW device [4]. On the other hand, the additional frequency doubler needs a strong input signal at 4.5 GHz (>1 mW). In this design, we decided for high harmonic power instead of a very low noise floor.

A near class C bias point leading to a conduction angle of about 120° allows efficient frequency doubling [5]. Starting with this bias point, the optimum load impedance was found by a harmonic load-pull technique similar to [6]. The transistor was measured under large signal operation with various load and bias conditions to get

(i) maximum second harmonic output,

(ii) at least 5 dB large-signal gain at the fundamental and

(iii) sufficient small signal gain (>7dB) at the fundamental for oscillator start-up.

Two optimum load impedances were found:

2.25GHz: $r_{L1}=0.74 \quad 120.5°$, $r_{L2}=0.74 \quad 8.4°$
4.5GHz: $r_{L1}=0.25 \quad 115.4°$, $r_{L2}=0.24 \quad 130°$

Load number 1, yielding slightly higher harmonic output power, was chosen.

3. Diplexer Network

The feedback network including the STW delay line presents these optimum load impedances to the second transistor and works as a diplexer filter. While the 2.25 GHz signal passes through the delay line, the 4.5 GHz signal is blocked and fed to the doubler. To minimize substrate area, a three port microstrip junction was used instead of a coupler or a wilkinson power divider. The 4.5 GHz output port is decoupled by a small resistive attenuator (4.5 dB).

4. Design of the Feedback Loop

The oscillator circuit doesn't include any tuning circuits for phase adjustments. To ensure the correct closed loop transmission phase and gain, the entire circuit was intensively modelled with a circuit simulation program (Touchstone). During these calculations, the feedback loop has virtually to be cut open. If the simulation introduces an impedance mismatch at the cutting point, the closed loop gain and transmission phase are not accurately predicted. To reduce these errors, the circuit of Fig. 4 was used for analysis and optimization of the loop gain and phase. Gain and transmission phase are calculated between points (1) and (2).

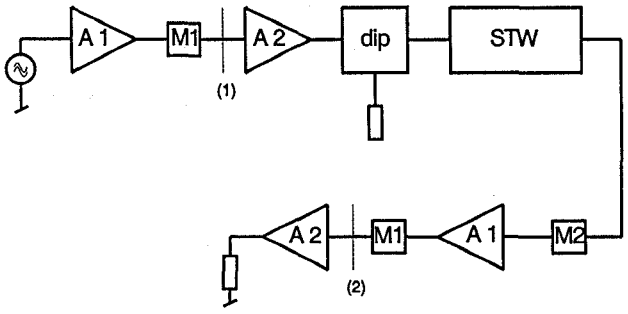

Figure 4: The circuit topology used for the computer simulation of the feedback loop

A1: linear amp. (1st stage)
A2: limiting amp. (2nd stage)
STW: STW delay line
dip: diplexer network
M1,M2: matching networks
(1),(2): input/output for analysis

The external impedances at both sides of the cutting point are approximated by a repetition of the circuit up to the first quasi unidirectional or high-loss element.

III. DESIGN OF THE OUTPUT FREQUENCY DOUBLER

The final doubler uses a GaAs FET (type NE710-83) because of its higher gain compared to bipolar transistors. An initial bias point of U_D = 3 V, I_{Do} = 2 mA, based on harmonics measurements in a 50 Ω system, was selected. (Biasing this FET near pinchoff gives a higher level of the second harmonic than a bias near I_{Dss} [7].) With the input power applied, self biasing increases the drain current, especially at P_{in} > 1 mW.

The optimum reflection coefficients were again determined from harmonic load-pull measurements. These measurements have shown that the input matching conditions have a strong influence on the optimum phase angle of the load reflection at the fundamental (4.5GHz).

The realized source and load reflection coefficients are as follows:

4.5GHz: r_S = 0.75 90° r_L = 0.88 90°
9.0GHz: r_S = not optim. r_L = 0.22 108°

Simulations with mwSPICE and the built-in Statz model [8] for the FET have shown good agreement with the load-pull measurements. The optimum phase angle of the load reflection at 4.5 GHz was between 50° and 70° in the simulation, compared to 90° from the measurement.
The measured conversion gain of the doubler alone is 5 dB with an input power of 1 mW.

IV. MEASUREMENTS

The oscillator is made on a 2" by 2" PTFE substrate (Epsilam 10). Fig. 5 shows a photograph of the complete circuit. On the right hand side, the feedback loop with the two transistors and the STW device can be seen. The output doubler is located at the left.

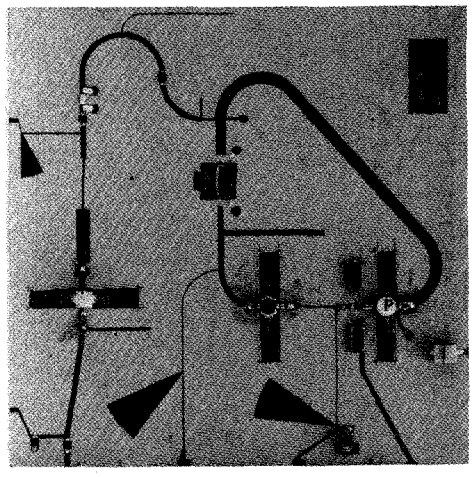

Figure 5: Photograph of the oscillator on the PTFE substrate

In this prototype, the source or emitter leads of the transistors are connected to the ground plane of the MIC by a two-piece displaceable fixture. To give an unobstructed view of the circuit, these fixtures have been removed, making the slots in the substrate visible.

The oscillator delivers 5 mW of output power at 9 GHz. The single sideband phase noise of the oscillator has been measured on a HP 3585 spectrum analyzer. For this measurement, the oscillator signal was downconverted using a HP 8340B synthesizer and a doubly balanced mixer.
The measurement limit of this setup is about -90 dBc/Hz at 10 kHz offset and -110 dBc/Hz at 100 kHz offset.

The resulting measurements of the phase noise close to the carrier are shown in Fig. 6 and 7.

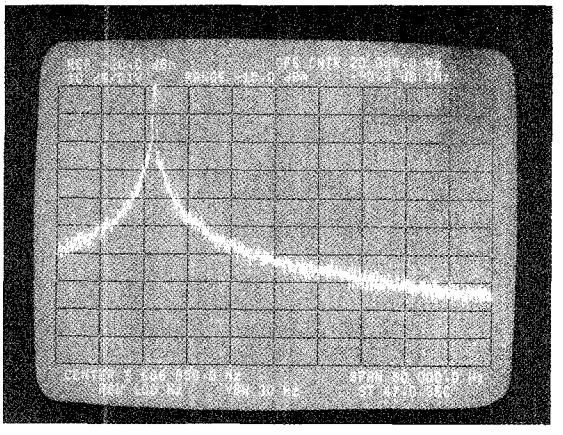

Figure 6: Phase noise of the 9 GHz STW oscillator at 20 kHz offset from the carrier

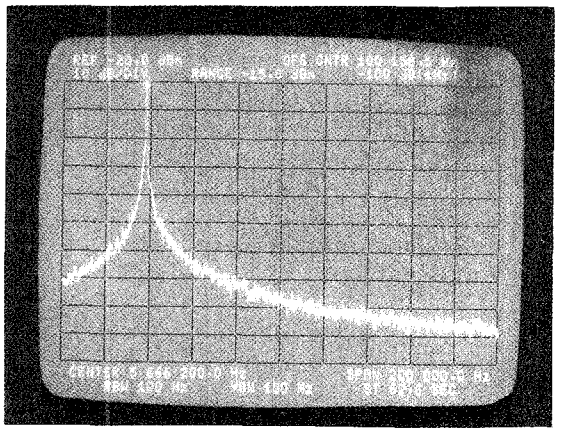

Figure 7: Phase noise at 100 kHz offset from the carrier (partially limited by the measurement system)

The phase noise is at least -90 dBc/Hz at 20 kHz and less than -108 dBc/Hz at 100 kHz offset. It was not possible to measure the far-away noise floor of the oscillator with the available equipment. The measured temperature drift is 0.6 MHz from 20°C to 70 °C.

CONCLUSIONS

The circuit is not optimized for low phase noise. Nevertheless it's performance is comparable to dielectric resonator oscillators. With overall dimensions of 2" by 2", the realized circuit is comparatively small. Because of the accurate calculation of the closed loop gain and phase, no phase adjustment in the feedback loop was necessary. The concept of the in-loop multiplier could also be applied to other kinds of feedback oscillators.

ACKNOWLEDGEMENTS

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